Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in this application.

Listing of Claims:

1. (Currently amended) An interface circuitry of a display chip, said interface circuitry comprising:

an input node for receiving an analog image signal with a display resolution;

a variable resistor electrically connected between said input node and an internal node;

a capacitor electrically connected between said internal node and a ground node;

[~~a filter for processing said analog image signal and providing a processed image signal at an internal node;~~] and

a switching device[~~clamping circuit~~] connected between said internal node and a reference level;

[~~wherein said filter provides a bandwidth adjustable in response to said display resolution such that the greater said display resolution, the greater said bandwidth;~~]

wherein said variable resistor and said capacitor form a filter for processing said analog image signal and providing a processed image signal at said internal node, and said switching device[~~clamping circuit~~] is used to clamp said internal node at a clamping voltage with reference to said reference level during a clamping interval.

2. (Canceled)

3. (Currently amended) The interface circuitry as claimed in claim 1, wherein said switching device is implemented by[~~clamping circuit comprises~~] a transistor connected between said internal node and said reference level.

4. (Original) The interface circuitry as claimed in claim 3, wherein said transistor is configured with a drain connected to said internal node, a source connected to said reference level and a gate controlled by a clamping signal.

5. (Canceled)

6. (Canceled)

7. (Currently amended) An interface circuitry of a display chip, said interface circuitry comprising:

an input node for receiving an analog image signal with a display resolution;

a first variable resistor electrically connected between said input node and an internal node;

a capacitor electrically connected between said internal node and a ground node;

a second variable resistor electrically connected to said internal node; and

[~~a filter for processing said analog image signal and providing a processed image signal at an internal node;~~

~~an ADC unit for converting said processed image signal into a digital image signal; and~~]

a switching device[~~clamping circuit~~] connected between said second variable resistor[~~internal node~~] and a reference level;

[~~wherein said filter provides a bandwidth adjustable in response to said display resolution such that the greater said display resolution, the greater said bandwidth;~~]

wherein said first variable resistor and said capacitor form a filter for processing said analog image signal and providing a processed image signal at said internal node, and said switching device[~~clamping circuit~~] is used to clamp said internal node at a clamping voltage with reference to said reference level during a clamping interval.

8. (Canceled)

9. (Currently amended) The interface circuitry as claimed in claim 7, wherein said switching device is implemented by[~~clamping circuit comprises~~] a transistor connected between said internal node and said reference level.

10. (Original) The interface circuitry as claimed in claim 9, wherein said transistor is configured with a drain connected to said internal node, a source connected to said reference level and a gate controlled by a clamping signal.

11. (Canceled)

12. (Canceled)

13. (Previously canceled)

14. (Previously canceled)

15. (New) The interface circuitry as claimed in claim 1, further comprising an ADC unit connected to said internal node for converting said processed image signal into a digital image signal.

16. (New) The interface circuitry as claimed in claim 1, wherein said filter provides a bandwidth adjustable in response to said display resolution.

17. (New) The interface circuitry as claimed in claim 7, further comprising an ADC unit connected to said internal node for converting said processed image signal into a digital image signal.

18. (New) The interface circuitry as claimed in claim 7, wherein said filter provides a bandwidth adjustable in response to said display resolution.

19. (New) An electronic circuitry, comprising:

a first capacitor for capacitively coupling an analog image signal to a first node;

a resistor electrically connected between said first node and a second node;

a second capacitor electrically connected between said second node and a ground node; and

a switching device connected between said second node and a reference level;

wherein said resistor and said second capacitor form a filter for processing said analog image signal and providing a processed image signal at said second node, and said switching device is controlled by a clamping signal to clamp said second node at a clamping voltage with reference to said reference level during a clamping interval.

20. (New) The electronic circuitry as claimed in claim 19, further comprising a variable resistor connected between said second node and said switching device.

21. (New) The electronic circuitry as claimed in claim 19, further comprising an ADC unit connected to said second node for converting said processed image signal into a digital image signal.

22. (New) The electronic circuitry as claimed in claim 21, further comprising a variable resistor connected between said second node and said switching device.

23. (New) The electronic circuitry as claimed in claim 19, wherein said switching device is implemented by a transistor.